AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions of claims in the application.

Listing of Claims:

1. (currently amended) An apparatus comprising:

~~a storage device to receive incoming~~ first-in, first-out buffer (FIFO) to strobe in data from a data source based on at least a first strobe signal or a second strobe signal, the strobe signals based on a bit transfer rate per strobe of the data source which is to be used to transfer the data to the FIFO, wherein the FIFO includes latches to latch in the data and output pairs of bits based on timing of the data bus; and

a select circuit to select between ~~a first strobe to strobe in the incoming data at a first strobe rate to transfer a first number of bits per strobe and a second strobe to strobe in the incoming data at a second strobe rate to transfer a second number of bits per strobe, the select circuit to select the first strobe or the second strobe based on a bit transfer rate per strobe of the data source~~ the strobe signals, including the first strobe signal and the second strobe signal, depending on the bit transfer rate per strobe of the data source, the first strobe signal to be selected when the data source has a first bit transfer rate per strobe and the second strobe to be selected when the data source has a second bit transfer rate per strobe.

2. (original) The apparatus of claim 1, wherein the select circuit is a multiplexer.

3. (original) The apparatus of claim 1, wherein the select circuit is to receive a select signal from a value stored in a register.

4. (original) The apparatus of claim 1 further including a register to store a programmable value used to select between the first and second strobes.

5-6. (canceled)

7. (currently amended) The apparatus of claim ~~5~~ 1, wherein the FIFO is comprised

of four latches to strobe in four bits of data and output a pair of bits onto the data bus during a first portion of a clock cycle and another pair of bits during a second portion of the clock cycle.

8. (currently amended) The apparatus of claim ~~5~~ 1 further including a second select circuit disposed in a data path of the incoming data to introduce delay in the data path to maintain phase relationship between the incoming data and the first or second strobe selected.

9. (currently amended) An integrated circuit comprising:

an interim first-in, first-out buffer (FIFO) ~~buffer~~ to strobe in data from a memory based on a first strobe signal or a second strobe signal, the strobe signals based on a bit transfer rate per strobe of the memory which is to be used to transfer the data to the FIFO; and

a select circuit to select between the first strobe signal and the second strobe signal depending on the bit transfer rate per strobe of the memory, the first strobe signal to be selected when the memory has a first bit transfer rate per strobe and the second strobe to be selected when the memory has a second bit transfer rate per strobe.

10. (original) The integrated circuit of claim 9, wherein the select circuit is a multiplexer.

11. (original) The integrated circuit of claim 10, wherein the multiplexer is to receive a select signal from a value stored in a register.

12. (original) The integrated circuit of claim 10 further including a register to store a programmable value to be used by the multiplexer to select between the first and second strobe signals.

13. (previously presented) The integrated circuit of claim 10, wherein the FIFO is comprised of latches to latch in the data and output pairs of bits onto an internal data bus

based on timing of the internal data bus.

14. (original) The integrated circuit of claim 10, wherein the FIFO is comprised of four latches to strobe in four bits of data and output a pair of bits onto an internal data bus during a first portion of a clock cycle and another pair of bits during a second portion of the clock cycle.

15. (original) The integrated circuit of claim 10 further including a second multiplexer disposed in a data path of the incoming data to introduce delay in the data path to maintain phase relationship between the incoming data and the first or second strobe selected.

16. (previously presented) A method comprising:

generating a plurality of strobes to accommodate data sources that have different bit transfer rates per strobe, in order to transfer data to a buffer at a bit transfer rate of a particular data source which is coupled to the buffer for data transfer;

selecting one strobe from the plurality of strobes to allow data transfer from the particular data source to the buffer at a bit transfer rate of the particular data source; and

receiving incoming data from the particular data source using the selected one strobe to receive the incoming data at the bit transfer rate of the particular data source.

17. (original) The method of claim 16 further including multiplexing the plurality of strobes and using a select signal for selecting the one strobe.

18. (original) The method of claim 17 further including delaying the incoming data to maintain phase relationship between the incoming data and the selected one strobe.

19. (original) The method of claim 18, wherein the receiving incoming data includes latching in the data and outputting pairs of bits based onto an internal data bus based on timing of the data bus.

20. (original) The method of claim 18, wherein the receiving incoming data includes latching to strobe in four bits of data and outputting a pair of bits onto an internal data bus during a first portion of a clock cycle and another pair of bits during a second portion of the clock cycle.